CELA-81
CONTROL BOARD
MANUAL

BALOGH

Notes are used to call attention to information that is significant to the understanding and operation of equipment.

This BALOGH manual is based on information available at the time of its publication. We have attempted to provide accurate and up-to-date information. This document does not purport to cover all details or variations in hardware or software; nor does it provide for every possible combination of products. Some features described herein may not be available on all like products. BALOGH assumes no obligation to notify holders of this document of any subsequent changes.

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MANUAL REVISION HISTORY

Revision Description	Latest Revision Date	Revision Number	Approval Date
Address Change	04/12/10	3	04/12/10

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Introduction

BALOGH's passive Radio Frequency Identification/Coding Systems identify pallets or products that carry a READ/WRITE TAG. The data carried by the TAG can be modified by a READ/WRITE system, which gives the user real-time access to production or quality control information. A system typically consists of a TAG, a Transceiver, a Control Board and a Control Board Holder. A more complete description of BALOGH Identification systems can be found in the ASSEMBLY MANUAL. The aim of this manual is to provide a description of the proper use, assembly, wiring and function of the CELA- 81 Control Board.

READ/WRITE TAGS

The OMA TAG stores, in its Ferro-Electric memory, data about the tagged item that is transmitted by the Transceiver. BALOGH TAGS are passive, meaning that the TAGS operate without an on TAG power source (Typically a battery with limited life). The TAG obtains all energy required from the Transceiver Transmission zone.

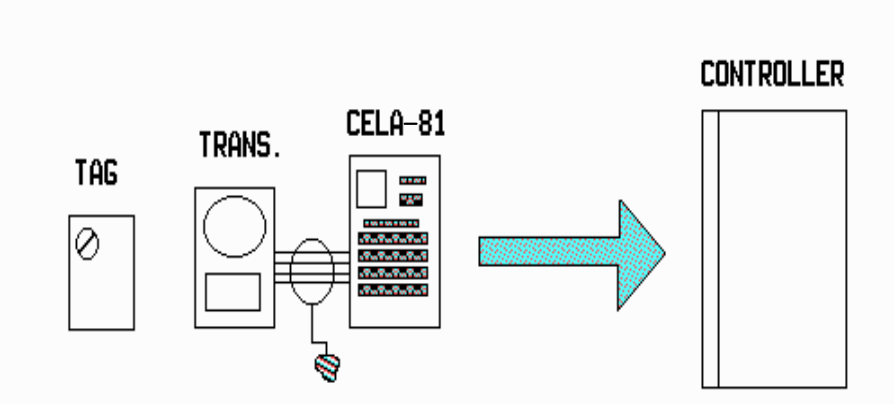
TAGS are available in a variety of memory capacities, 64 x 8 bits, 2K x 8 bits, and 8K x 8 bits. All OMA TAGS have unlimited READ and 10 billion WRITE cycle capability and are warranted for 5 years under normal operating conditions. The TAGS can be used in very harsh industrial environments such as wash cycles and paint applications. The TAGS are unaffected by water, oil, detergents, metal chips or intense electro-magnetic fields, and are engineered for such applications.

TRANSCEIVERS

The Transceivers are available in many styles with varying transmission ranges. It is the Transceiver that provides the electro-magnetic energy necessary to power the TAG, hence the term 'passive'. Aside from energy emission, the Transceiver is also the conduit for data transmission and data reception. In order to perform a READ or WRITE, the transceiver must be wired to a BALOGH Control Board. The Control Board is the interface between the user's logic system and the RF TAG / Transceiver communications.

Choosing a BALOGH RFID system is an application driven process. Answering the following questions will help to narrow the choices for the appropriate Transceiver.

- What is the READING/WRITING distance necessary between the TAG and Transceiver?
- What are the distances between READING/WRITING stations?
- Which Transceiver shape best suits the application and mounting constraints?
- Which TAG shape best suits the application and mounting constraints?
- What is the communication speed requirement of the TAG? (in on-the-fly READING/WRITING applications)
- What are the transmission zone dimensions needed



CELA-81 Control Board

- Micro programmable Euro-style Board;
- Multiplex able parallel connection;
- Acts as an interface between the user's logic device and the BALOGH Transceivers and TAGS;
- Writes to the TAG byte by byte from the data received on its parallel inputs;
- Responds, on its parallel outputs, with the data read from an address in the TAG;
- Each Transceiver must be connected to a CELA-81;
- Multiple CELA-81 Boards can be connected to create a network that reduces the number of PLC inputs and outputs (data line multiplexing).
- Echoes instructions received from the users logic device (i.e., PLC).

OPERATION OF THE CELA-81

The CELA-81 is connected to a Host Controller (PLC, PC etc.) via parallel I/O and functions as a TAG interface.

READING or WRITING to a TAG takes place in two stages.

Stage 1: BOARD PROGRAMMING
The CELA-81 receives, on its inputs, instructions from the user's programmer: 1) The byte address to be read or written and the READ or WRITE command; 2) If writing to a TAG, the data to be written is entered. At this programming stage, the presence of the TAG is not necessary. A full description of this stage is presented in sections 4 and 5 of this manual.

Stage 2: TAG READING OR WRITING
Stage 2 involves the actual READING or WRITING of a TAG. As the TAG enters into the Transceiver's field, dialogue takes place automatically. Successful completion of the operation is verified when the CELA-81 signals a valid operation (VAE or VAL).

Inputs and Outputs

INPUTS TO CELA-81
BUS I (parallel line, 8 bits, I0-I7)

DCY - SELECTION AND STORAGE INPUT
INPUT FROM THE TRANSCEIVER
SBA - MULTIPLEXING INPUT
POWER SUPPLY

OUTPUTS FROM CELA-81
BUS O (parallel line, 8 bits, O0-O7)

TRANSCEIVER ERROR INDICATOR
VAL - READ VALIDATION
VAE - WRITE VALIDATION
PRE - TAG PRESENCE
DEFB - BATTERY DEFAULT

INPUT BUS

The CELA -81 uses an 8-bit input bus that serves a dual purpose. When the DCY logic line is in the low state, the Input Bus is recognized as an address and READ/WRITE command bus; using bits 0 - 5 for addressing, and using bit 7 to select READ or WRITE mode.

When the DCY line is in the high state, the Input Bus is recognized as a DATA Input Bus for storing the DATA that will be written to the TAG when the write mode has been selected.

	LSB (Least Significant Bit)							MSB (Most Significant Bit)
BUS I	I0	I1	I2	I3	I4	I5	I6	I7
ADDRESS	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	--- ---	0=READ 1=WRITE
DATA	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7

DCY COMMAND

This input enables the programming of a READ or WRITE operation.

SWITCHING FROM LOGIC 0 TO LOGIC 1: This action stores the address currently on the Input Bus plus the READ or WRITE command (I7 status).

DCY at logic 1: The CELA-81 echoes the address and read/write command presented to the CELA-81's Input Bus (on the Output Bus). The CELA-81 will not dialogue with a TAG.

VAL and VAE status lines will assume the following states:
When READING: **VAL** 1 switches to 0, VAE remains at logic 1
* When WRITING: **VAE** 1 switches to 0, VAL remains at logic 1

* If writing to a TAG, enter data on the CELA-81's Input Bus BEFORE switching DCY to logic 0.

SWITCHING FROM LOGIC 1 TO LOGIC 0:

DCY at logic 0:

When READING: All bits of the OUTPUT BUS are set to logic 0 until the TAG is READ.
Transmitting and receiving between the CELA-81 and a TAG is enabled.
Upon successful completion of a READ operation, the data will be presented on the CELA-81's Output Bus.

When WRITING: The byte to be WRITTEN is stored in memory.
All bits of the OUTPUT BUS are set to logic 0.
Transmitting and receiving between the CELA-81 and a TAG is enabled.
Upon successful completion of a WRITE operation, the data written will be echoed on the CELA-81's Output Bus.

SBA COMMAND

This input is used when multiplexing the data lines of two or more CELA-81 Control Boards.

SBA = 1: CELA-81 selected. The board can dialogue with the user and the TAG.
SBA = 0: CELA-81 status lines are active (PRE, VAL, VAE DEFB).
CELA-81 can dialogue with the TAG.
INPUT BUS disabled.
DCY disabled.
OUTPUT BUS high impedance.

OUTPUT BUS

The Output Bus has 8 parallel outputs and displays two kinds of data.

1) When the DCY logic line switches from logic 0 to logic 1, the data present on the Output Bus is an echo of the address and READ/WRITE command status that is currently on the Input Bus.

2) When the DCY logic line switches Logic 1 to Logic 0 and a TAG is present for dialogue, the data present on the Output Bus can be interpreted two ways. If the CELA-81 is in READ mode, the data present on the Output Bus is data read from a TAG. If the CELA-81 is in WRITE mode, the data present of the Output Bus is an echo of the data written to the TAG.

PRE STATUS OUTPUT

When a TAG enters the field of the Transceiver the PRE Status Output switches to logic 1. This indicates that a TAG has entered the transmission zone and its microprocessor has been reset and is now able to be either READ or WRITE.

When a TAG leaves the transmission zone of the Transceiver the PRE Status Output switches to logic 0. Additional communication cannot take place.

The PRE output can be effectively used to indicate presence of the TAG and/or pallet carrier. This output works independently of any programming.

VAL STATUS OUTPUT

The VAL logic line is an absolute indication that the data present on the output bus is correct data. This line should always be used in the program logic to confirm that the output Bus has settled and that the data is correct.

When the DCY switches from logic 0 to logic 1, storing the address and read command found on the Input Bus (BUS I), VAL switches to logic 0. It is now ready to accept and display valid reads.

It is important to verify that VAL has switched to logic 0 before proceeding with the next programming stage. This insures that the board has understood the programming.

The VAL will switch from logic 0 to logic 1 in three cases:

- When a satisfactory READ operation has been completed. The word that was read will now be available on the Output Bus (BUS O).
- If the user requests a WRITE operation by toggling DCY and causing it to switch from 0 to 1.
- If the user cancels the program (using manual or logical reset), the VAL will transition to Logic 1 and VAE will be at Logic 1.

The VAL signal could appear up to 25 ms after the data arrives on the output bus. Therefore, no data should be assumed correct until the VAL has returned a Logic 1 as confirmation.

VAE STATUS OUTPUT

When the DCY switches from logic 0 to logic 1, storing an address and a WRITE order (found on BUS I), the VAE switches to logic 0. It is now ready to accept and display valid writes.

It is important to verify that the VAE has switched to logic 0 before proceeding with the next programming stage. This insures that the board has understood the programming.

The VAE will switch from logic 0 back to logic 1 in these three cases:

- When a satisfactory WRITE operation has been performed. The word that was written will now be available on the Output Bus (BUS O).
- If the user requests a READ operation by toggling the DCY and causing it to switch from logic 0 t1.
- If the user cancels the program (using manual or logical reset), the VAE will transition to Logic 1 and VAL will be at Logic level 1.

DEFB STATUS OUTPUT (Only applies when using older semi-passive TAGS)

The DEFB is normally on logic 0.

If the battery has reached its loss of power threshold and needs to be replaced, the DEFB (default battery) status line will show logic 1. (This does not affect data integrity, and READING/WRITING may still occur.) If the battery is not replaced, the TAG will eventually lose its ability to back up memory. After replacing the battery, reinitialize the TAG memory.

TRANSCEIVER ERROR OUTPUT

The TR ERR is normally on logic 0

This output indicates the existence of any faults in the Transceiver wiring. This output will show logic 1 if any of the following conditions occur:

- If the Transceiver is improperly wired;
- If any wire is cut;
- If a ground fault occurs.

This output will be reset to zero when the fault is corrected and:

- A TAG appears in the Transceiver's transmission zone
- The CELA-81 is reprogrammed.

CELA Operations

READING A TAG

Stage 1: CELA-81 Programming

1) Set SBA to logic 1. This selects the target board.
2) Set I7 of the CELA-81 Input Bus to logic 0 (see 3.1).
3) Set desired address using Input Bus. For example, to set address 7 in the TAG, set bits I0, I1 and I2 to Logic 1 (i.e., 1, 1, 1, 0, 0, 0).
4) Switch DCY from 0 to 1.
   DCY at logic 1:
   - Stores READ address in memory;
   - VAL switches from logic 1 to logic 0;
   - Echoes on the Output Bus the address present on inputs.
5) Switch DCY from 1 to 0, which results in:
   - clearing of the OUTPUT Bus;
   enabling dialogue with the TAG.

NOTE: During Stage 1 the presence of a TAG in the Transmission zone is not necessary

Stage 2: This stage is invisible to the user. The CELA-81 reads the TAG memory at the indicated address and performs an absolute data check.

Stage 3: This is the reporting stage. The CELA-81 presents the data read to its Output Bus (BUS O). After a time delay "tVAL" the CELA-81 switches its VAL output to logic 1. Data has been latched on the Output Bus.

WRITING TO A TAG

Stage 1: CELA-81 Programming

1) Set SBA to logic 1. This selects the target board.
2) Set I7 of the input bus (BUS I) to logic 1. (See 3.1)
3) Set desired address using BUS I. For example, to set address 43, set bits I1, I2, I4 and I6 to Logic level 1 (i.e., 1, 1, 0, 1, 0, 1).
4) Switch DCY to logic 1 from logic 0. This will result in:
   - The Storage of write address in memory;
   - VAE switching from logic 1 to logic 0.
   - Echo of stored address and write command on BUS O.

PROGRAM 5) Set any desired data value on BUS I; (by using all 8 bits, numeric values 0 to 255 are possible).
6) Switch DCY 1 to 0, which results in:
   - storage of the data present on BUS I;
   - clearing of BUS O (when no TAG is present);
   - enabling of dialogue between the CELA-81 and the TAG.

Stage 2: This stage is invisible to the user. When the TAG enters the transmission zone:
   - Output PRE switches to logic 1;
   - The address and the data stored by the CELA-81 are transmitted to the OMA (writing);
   - The TAG stores the data and echoes it on the CELA-81; and
   - The CELA-81 verifies the data for absolute data accuracy.

Stage 3: This is the reporting stage. The CELA-81 presents the data written directly to its Output Bus (BUS O). After a time delay "tVAL" the CELA-81 switches its VAE output to logic 1. The CELA-81 is then latched and waits for further instructions.

IMPORTANT NOTE:

So long as a TAG is not in the field of the Transceiver, the user can reprogram the CELA-81 at the end of stage.

ON-THE-FLY READING OR WRITING

When READING or WRITING on-the-fly, CELA-81 programming does not change in any way.
See Chapter 3 in the ASSEMBLY MANUAL for details concerning READING or WRITING to a TAG in motion.

MULTIPLEXING

This feature enables the user to access any one of multiple CELA- 81 Control Boards connected to the same I/O rack in the user's logic unit (PLC). The SBA control line is used to select the board.

ONLY ONE CELA-81 AT A TIME CAN BE SELECTED (i.e., SBA = LOGIC 1) ALL OTHER BOARDS MUST BE DESELECTED (i.e., SBA = LOGIC 0)

For the characteristics of the SBA = Logic 1 and SBA = Logic 0 see section entitled SBA COMMAND (3.3). The CELA-81 can be pre-programmed then deselected by the host. The programmed operation will occur, independent of the host, when a TAG arrives. The board's status lines signal the current activity of the board.

EXAMPLE

OBJECTIVE: Select a target CELA-81 as a TAG enters the transmission zone of its Transceiver.
PROGRAMMING SEQUENCE:

The TAG arrives.
PRE output switches to logic 1 and the appropriate validation output occurs (VAL or VAE). Data is verified by the CELA-81.
At this point, switching the SBA to logic 1 selects the CELA-81. (SBA = 1)
BUS O outputs the READ or WRITTEN word.
VAE and VAL are now at logic 1.

(See also wiring diagram on page 13, **Multiplexing several CELA-81 Boards**)

MULTIPLEXABLE I/O	NOT MULTIPLEXABLE I/O	
BUS I	SBA	PRE
DCY	VAL	DEFB
BUS O	VAE	TR ERR

RESET AND INITIAL CONDITIONS

The CELA-81 can be reset manually or through the PLC. When the board is reset the following occurs:

- ! Any programmed instruction is cleared
- ! The Input Bus is disregarded
- ! The Output Bus is cleared
- ! VAL and VAE are both at logic 1
- ! PRE if active, is not affected
- ! TR ERR if active, is not affected

For manual reset, simply press the Reset button on the Control Board.

PLC reset: If the board is programmed and DCY is still on logic 1, set SBA input line at logic 0. This will cancel any programmed function.

If power is lost, cycled, or drops below acceptable levels, the board will restore itself to the above reset conditions when the proper power has been restored.

INITIALIZING THE TAG WITH THE CELA-81

If the battery is removed from a TAG or the battery back up has dropped below its proper support level, the TAG may "go to sleep" meaning -- it can't be read. If this occurs, the user must install a new battery and write to the TAG using the CELA-81.

Note: Current TAG models do not require a battery.

This operation is easily accomplished with the Hand-Held PM-15 READ/WRITE Unit. Trouble shooting and debug time is greatly reduced with this portable READER/WRITER. Please inquire at the factory for price and delivery 800-252-RFID.

TROUBLE SHOOTING TIPS

PROBLEM: The DCY control line is strobed but no echo occurs, and the board will not accept programming.

SOLUTION: If it is a dedicated board, i.e., the data lines are not being multiplexed; verify that the Control Board has the SBA (multiplexing line) tied high.

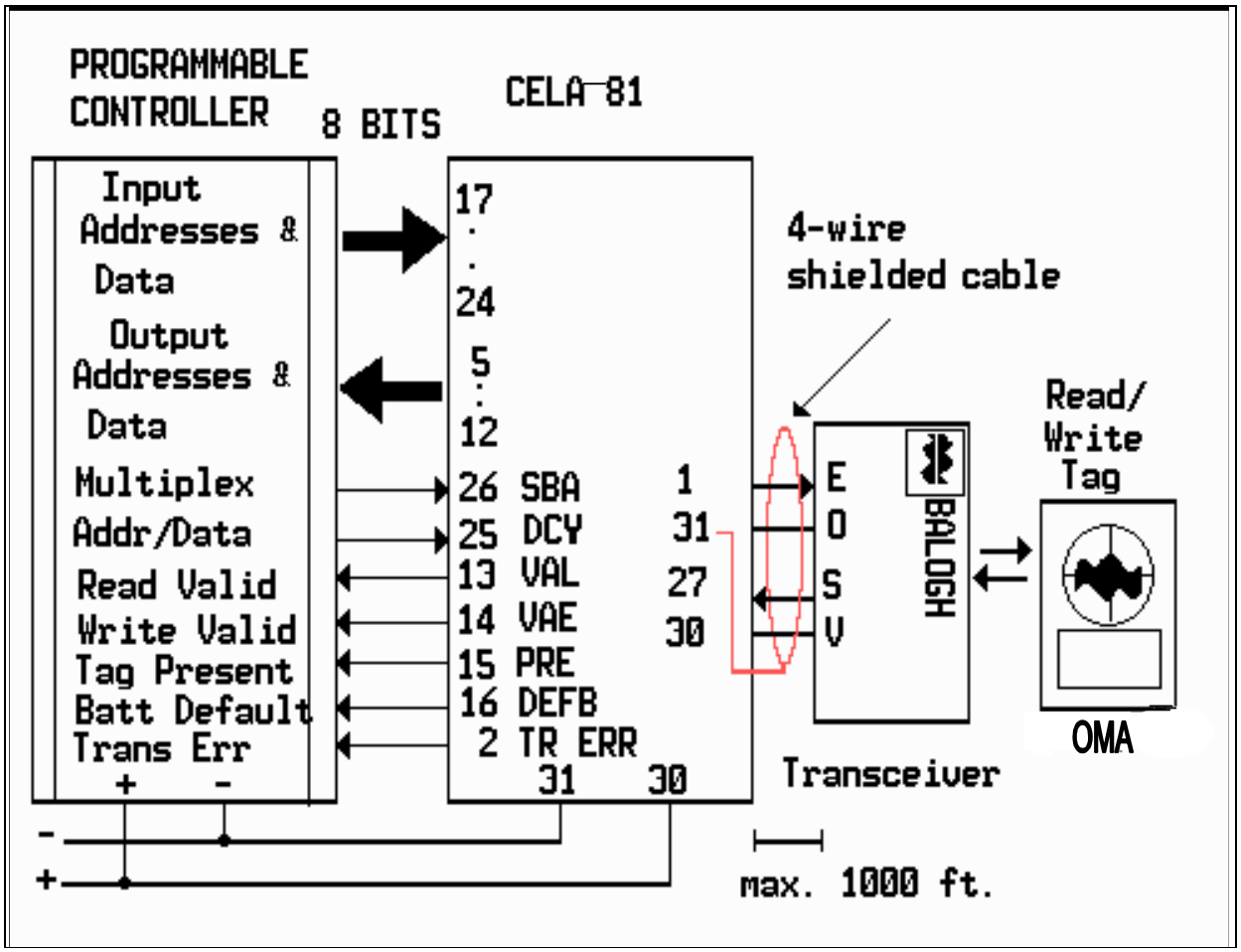
SOLUTION: If the board is multiplexed, be sure that the SBA control line has been brought high before programming begins.

SOLUTION: Verify that the DCY pulse is held high long enough for the CELA-81 to acknowledge your programming operation.

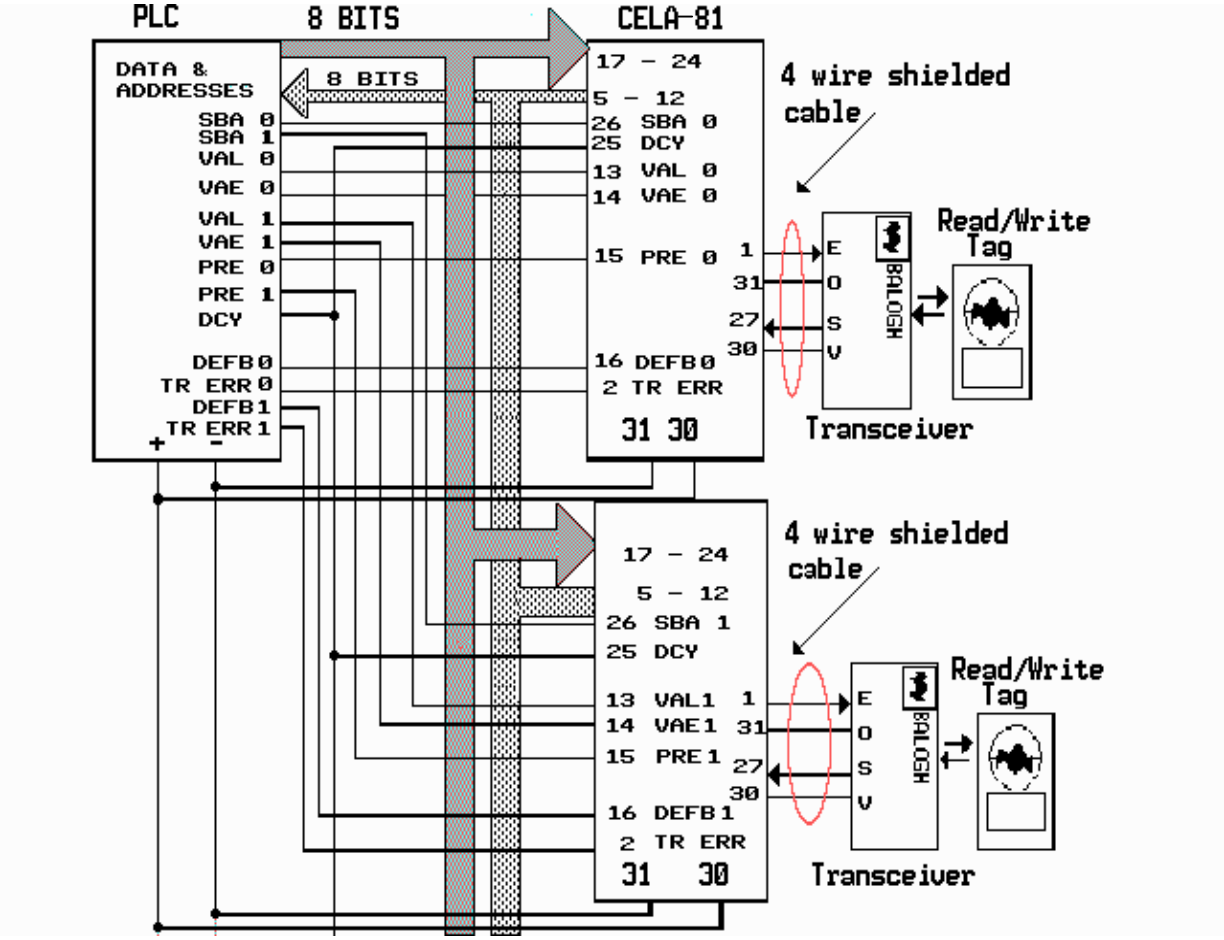
Wiring A CELA-81

CELA INPUTS TERMINALS
Power supply (+24V) DC: 30
Serial input from the trans: 27
SBA Multiplexing input: 26
DCY selection and storage input: 25
BUS I(parallel link, 8 bits, I0-I7):
Terminals 17-24; 17(2^7) = Most Sig Bit

CELA OUTPUTS TERMINALS
Serial output to trans: 1
VAL read validation: 13
VAE write validation: 14
PRE TAG presence: 15
BUS O (parallel link,8 bits O0-O7):
Terminals 5 - 12; 5(2^7) = Most Sig Bit
DEFB Battery Default : 16
TR ERR Transceiver Error: 2



Multiplexing several CELA-81 Boards



CELB-81

The CELB-81 Control Board READS or WRITES groups of individually addressable data. Several blocks of data at discontinuous addresses can be read or written during the course of one PLC scan. A READ/WRITE system using CELB-81 Control Board will READ and/or WRITE to BALOGH TAGS with memories of 64 bytes, 2 K-bytes or the first 2 K-bytes of an 8 K-bytes TAG.

Advantages:

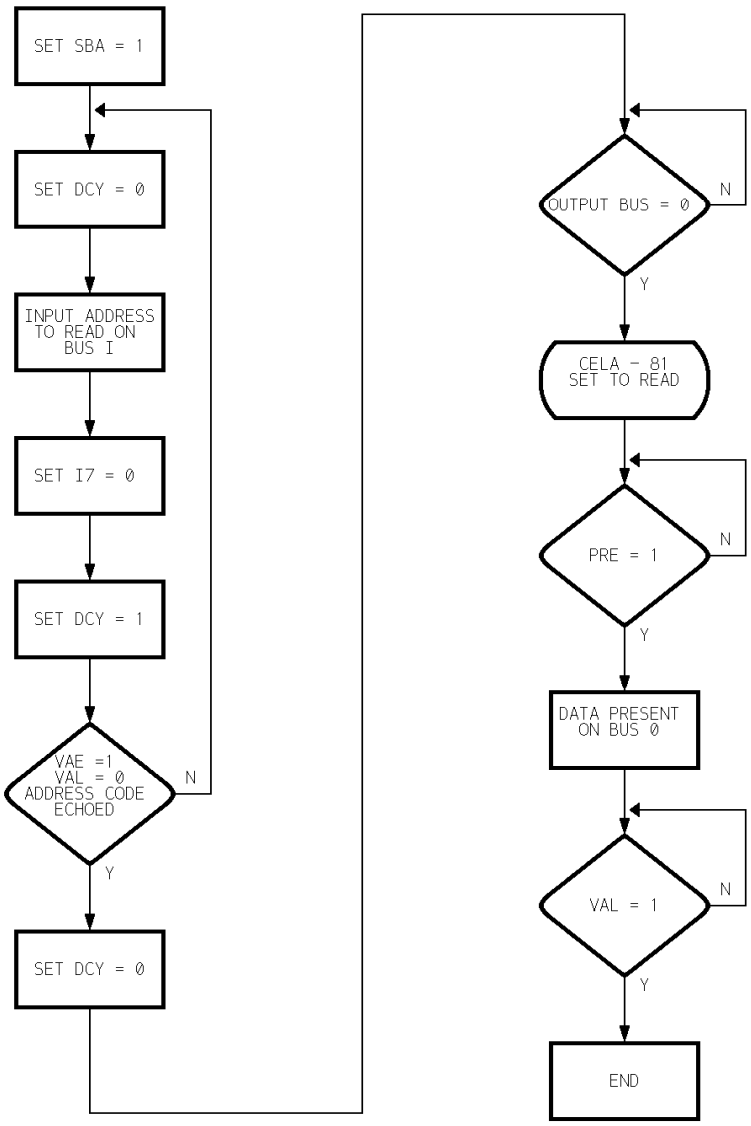
- Board can be preprogrammed by the PLC to execute multiple READS or WRITES when a TAG enters the transmission zone.
- Increases throughput time.
- Reduces instruction-loading time.
- Reduces data acquisition time.
- Saves all acquired data when the TAG leaves the zone.
- READS and WRITES at the same speed.
- 1 inputs: 8 for address/data (Input Bus I0 to I7); 3 for CONTROL.
- 14 outputs: 8 for address/data (Output Bus O0 to O7); 6 for STATUS.
- Maintains absolute data integrity.

TIMING TABLE (In milliseconds)

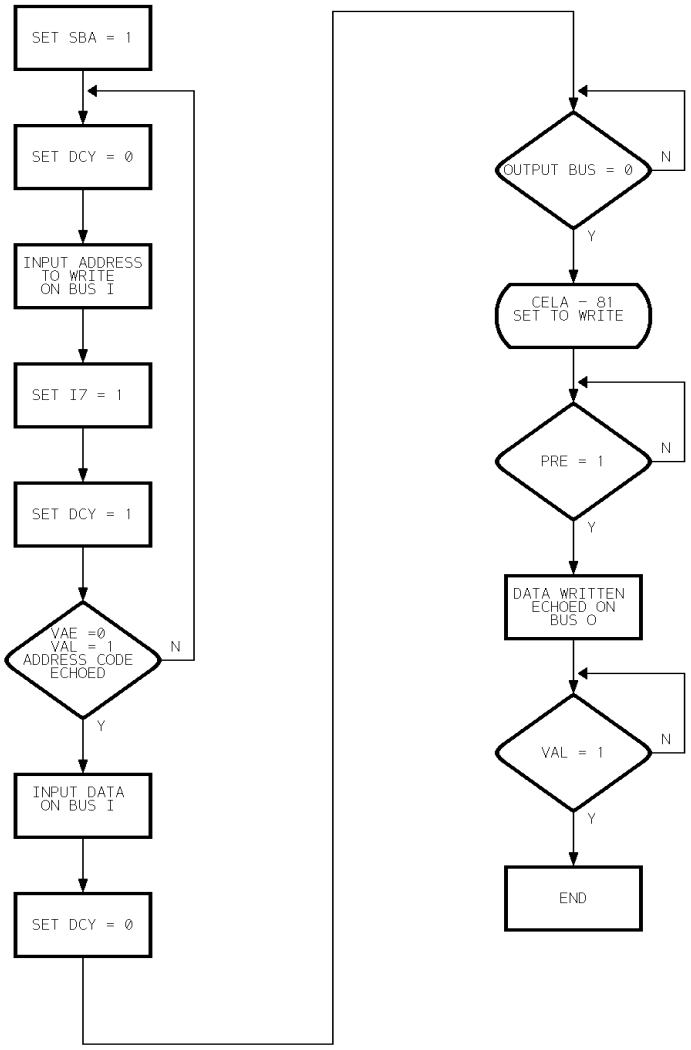
SYMBOL	MIN.	MAX.	DEFINITIONS
tSBAS		100	SBA/OUTPUTS response time
tANL		150	VAL/VAE response time upon validation
tDCYS		100	DCY/OUTPUTS response time
tOMA	50		DIALOGUE TIME. BUS O /PRE delay
tVAL	25		Delay at rise of VAL/VAE/BUS O
tME	100		BUS I Input hold time
tSBAE	100		Delay at fall of SBA/DCY in WRITING
tSBAL	0		Delay at fall of SBA/DCY in READING
tMEV	0		BUS I hold time/fall of VAL VAE
tDCYE	0		Delay at rise of DCY/BUS I
tSBAY	0		Delay at rise of DCY/SBA

FLOW CHARTS

PROGRAMMING FLOW CHART FOR A BYTE READ OF CELA-81



PROGRAMMING FLOW CHART FOR A BYTE WRITE OF CELA-81

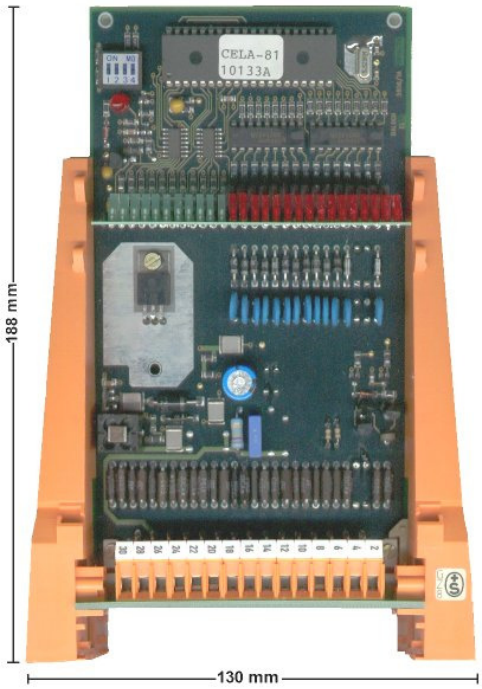


Control Board CELA-81

Identification - Coding

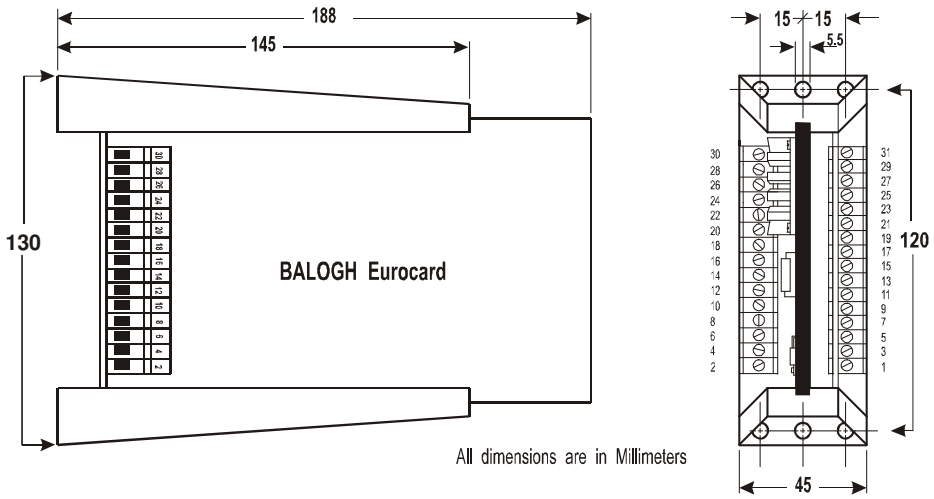
Characteristics

- Parallel Control Card, Eurocard Format (100 x 160mm)
- Multiplexable parallel connection
- Allows Reading and Writing of type “OMA” 64 byte TAGS.
- Each Control Board must be connected to a BALOGH Transceiver in order to Read/Write data from the TAGS.
- Requires GC-01 Board Holder



Characteristics at 25° C	Symbol	Unit	CELA-81
V Supply (< 2% Ripple)	Vcc	V DC	24
VolTAGe Tolerance			-10% to +10%
Current Consumption	Im	MA	150
Serial Connection			No
No. of Parallel Inputs			10
Input Impedance	Ze	K ohm	10
Input Logic 0		V	0 to 10
Input Logic 1		V	15 to Vcc
No. of Parallel Outputs			13
MAX Continuous Current (per Output)	Is	Ma	100
MAX VolTAGe Drop across an Output	Vdrop	V	1.5
Output Logic 0		V	0
Output Logic 1		V	Vcc – 1.5
MIN Ambient TEMP	Tmin	℃	0
MAX Ambient TEMP	Tmax	℃	+70
Protection Degree	IP		00
Weight	M	g	300
MAX Cable Length Between Control Board and Transceiver			1000 ft
MAX Cable Length Between Control Board and Buffer			
Short Circuit Protected			Yes
Protected against Inverse Polarity			Yes

CELA-81 Control Board



Terminal	Locations	ER*71/85	ER*80
1	Transceiver Output Connected to	E	Term 3
2	Transceiver error Output		
3			
4			
5	Bit 7 Output (MSB)		
6	Bit 6 Output		
7	Bit 5 Output		
8	Bit 4 Output		
9	Bit 3 Output		
10	Bit 2 Output		
11	Bit 1 Output		
12	Bit 0 Output (LSB)		
13	VAL Output		
14	VAE Output		
15	PRE Output		
16	DEFB Output		
17	Bit 7 Input (MSB)		
18	Bit 6 Input		
19	Bit 5 Input		
20	Bit 4 Input		
21	Bit 3 Input		
22	Bit 2 Input		
23	Bit 1 Input		
24	Bit 0 Input (LSB)		
25	DCY Input		
26	SBA Input		
27	Transceiver Input Connected to	S	Term 2
28			
29			
30	+24 VDC to Board & Transceiver	V	Term 1
31	Ground	O	Term 4

Note: When using a BALOGH Transceiver Cable V is Brown, S is White, E is Blue and O is Black.